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10/735,899	12/16/2003	Atsuhiro Otaka	032172	5713

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WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
TRUONG, LOAN	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,899	OTAKA ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-11,13,15-19,21 and 23-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,27 and 28* is/are allowed.

6)☒ Claim(s) *1, 3, 5-6, 8-11, 13, 15-19, 21, 23-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to applicant's reply filed November 16, 2006.

2. Claims 1, 3, 5-11, 13, 15-19, 21 and 23-31 are presented for examination. Claims 1, 3, 6-8, 11, 13, 16, 19, 21 and 24 have been amended. Claims 2, 4, 12, 14, 20 and 22 are cancelled. Claims 27-31 are newly added.

Response to Arguments

3. Applicant's arguments filed November 16, 2006 with respect to claim 1, 11 and 19 have been considered but are moot in view of the new ground(s) of rejection.

However, examiner would like to acknowledge that in regard to claim 1, 11 and 19, applicant stated that Lin does not teach the limitations of switching to the memory in standby when the BIOS cannot be booted. As stated in the first office action, Lin does disclosed the method of not receiving the confirmation signal by the BIOS switching circuit before the delay signal thereby assuming that the primary BIOS is corrupted (*interpreted to equate to cannot be booted)* and set the MHINIT low and BHINIT high to shadow the secondary BIOS program into the predetermined CPU address space to begin executing the secondary BIOS programs after the reset operation (*paragraph 0029).* Lin switched to the secondary BIOS by assuming that the primary BIOS is corrupted and load the secondary BIOS program into the predetermined CPU address space to be booted after the reset operation.

In regard to the newly added claims, refer to 35 U.S.C. 102(e) as being anticipated by Cepulis et al. (US 2004/0025002).

Allowable Subject Matter

4. Claims 7 and 27 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The examiner deems claims 7 and 27 as novel when read as a whole for the limitations of a redundancy management method for BIOS comprising the steps of: preventing execution of said switching when said hardware is started up for power recovery.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 28 is rejected to because of the following informalities: The period on line 9 of claim 28 should be replace by a semicolon. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 3, 5-6, 8-11, 13, 15-19, 21, and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 2002/0099974) in further view of Tamori et al. (US 5,960,445).

In regard to claim 1, Lin disclosed a redundancy management method for BIOS, comprising the steps of: using one of a pair of memories, which respectively store the BIOS for setting hardware in an environment in which OS can use said hardware, for operation and the other for standby (*Primary BIOS and Secondary BIOS, fig. 1A)*;

switching to the BIOS in said memory in standby when the BIOS in said one memory cannot be booted (*Confirmation signal not received, then shadow secondary BIOS, fig. 2)*; and

Lin does not explicitly teach a redundancy management method for BIOS comprising the steps of: executing an update of said BIOS by writing to said memory in standby; permitting switching said memory in standby to in operation when the update of said BIOS in said memory in standby succeeded; and writing the BIOS of said memory switched to operation to said memory switched to standby for redundancy after said switching.

Tamori et al. disclosed the method of updating a program and information processing system by configuring a flash ROM board as two banks A and B (*col. 5 lines 49-55).* Updating a BIOS in the flash ROM board, is described in fig. 8, utilizing the flash ROM board with two banks and the bank change circuit (*fig. 6, 92, col. 6 lines 11-17)* where the new BIOS is supplied from the network interface card to the RAM (*fig. 8, s9, col. 6 lines 35-39)* and the content of RAM is then written to bank A (*fig. 10-18).*

It would have been obvious to modify the method of Lin by adding Tamori et al. method of updating a program and information processing system. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would enable the BIOS to be immediately reinstalled if writing of a new BIOS ends in failure and to prevent the old BIOS from being lost by an operation error (*col. 2 lines 16-24).*

In regard to claim 3, Lin disclosed the redundancy management method according to claim 1, further comprising a step of switching said permitted memory in standby to in operation, and said memory in operation to in standby when said hardware is started up (*set the GPIO2 register to a value that will place a value on the selection signal line indicates usage of the secondary BIOS program, fig. 3, 206, paragraph 0038).*

In regard to claim 5, Lin disclosed the redundancy management method for BIOS according to claim 1, further comprising a step of preventing switching of said memory in standby to said memory in operation when the update of said BIOS in said memory in standby

failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 6, Lin disclosed the redundancy management method for BIOS according to claim 1, further comprising a step of preventing switching said memory switched to standby, to said memory in operation when writing of said BIOS in said memory switched to standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 8, Lin disclosed the redundancy management method for BIOS according to claim 1, further comprising a step of preventing execution of said redundancy step when said hardware is started up for power recovery (*secondary BIOS program may be overwritten by a copy of the functional primary BIOS in recovery operation, paragraph 0050).*

In regard to claim 9, Yang et al. disclosed the redundancy management method for BIOS according to claim 1, further comprising a step of executing the update of BIOS in a memory in standby of another hardware connected with said hardware according to the update of the BIOS in said memory in standby of said hardware (*recovery of BIOS by overwritten the secondary BIOS with a copy of the functional primary BIOS, paragraph 0050).*

In regard to claim 10, Yang et al. disclosed the redundancy management method for BIOS according to claim 1, further comprising a step of executing the synchronization

processing of the BIOS with another hardware connected with said hardware (*pure copying operation performed to place an identical copy of the primary BIOS into secondary BIOS, paragraph 0050).*

In regard to claim 11, Yang et al. disclosed a data processing apparatus, comprising:

a hardware including a CPU (*fig. 1A, 20)*;

a pair of memories which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware (*primary BIOS and secondary BIOS, fig. 1A, 40p, 40s)*; and

a service processor for using one of said pair of memories for operation and the other for standby (*Primary BIOS and Secondary BIOS, fig. 1A)* when said hardware is started up and switching to the BIOS in said memory in standby when the BIOS of said one memory cannot be booted (*Confirmation signal not received, then shadow secondary BIOS, fig. 2)*,

Lin does not explicitly teach a data processing apparatus wherein said CPU executes the update of said BIOS by writing to said memory in standby; wherein said service processor permits switching said memory in standby to said memory in operation when the update of said BIOS in said memory in standby succeeded, and wherein said CPU writes the BIOS of said memory switched to operation, to said memory switched to standby for redundancy after said switching.

Tamori et al. disclosed the method of updating a program and information processing system by configuring a flash ROM board as two banks A and B (*col. 5 lines 49-55).* Updating a BIOS in the flash ROM board, is described in fig. 8, utilizing the

flash ROM board with two banks and the bank change circuit (*fig. 6, 92, col. 6 lines 11-17)* where the new BIOS is supplied from the network interface card to the RAM (*fig. 8, s9, col. 6 lines 35-39)* and the content of RAM is then written to bank A (*fig. 10-18).*

Refer to claim 1 for motivational statement.

In regard to claim 13, Lin disclosed the data processing apparatus according to claim 12, wherein said service processor switches said permitted memory in standby to a memory in operation, and said memory in operation to said memory in standby when said hardware is started up (*primary BIOS has detected internal errors and BIOS switching circuit shadow in the secondary BIOS program, paragraph 0034).*

In regard to claim 15, Lin disclosed the data processing apparatus according to claim 11, wherein said CPU prevents switching said memory in standby to the memory in operation when the update of said BIOS in said memory in standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 16, Lin disclosed the data processing apparatus according to claim 11, wherein said CPU prevents switching said memory switched to standby, to said memory in operation when writing of said BIOS in said memory switched to standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must*

continue to be used, fig. 3, 205, paragraph 0037).

In regard to claim 17, Lin disclosed the data processing apparatus according to claim 11, further comprising another hardware connected with said hardware, and said hardware executes the update of the BIOS in the memory in standby of said other hardware connected with said hardware according to the update of the BIOS in said memory in standby of said hardware (*recovery of BIOS by overwritten the secondary BIOS with a copy of the functional primary BIOS, paragraph 0050).*

In regard to claim 18, Lin disclosed the data processing apparatus according to claim 11, wherein said hardware executes the synchronization processing of the BIOS with said other hardware connected with said hardware (*pure copying operation performed to place an identical copy of the primary BIOS into secondary BIOS, paragraph 0050).*

In regard to claim 19, Lin disclosed a storage system, comprising: a storage control apparatus comprises:

a hardware including a CPU (*fig. 1A, 20)*;

a pair of memories which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware (*primary BIOS and secondary BIOS, fig. 1A, 40p, 40s)*; and

a service processor for using one of said pair of memories for operation and the other for standby (*Primary BIOS and Secondary BIOS, fig. 1A)* when said hardware is started up and

switching to the BIOS in said memory in standby when the BIOS of said one memory cannot be booted (*Confirmation signal not received, then shadow secondary BIOS, fig. 2)*; and

a plurality of storage devices (*flash ROM to hold primary and secondary BIOS program, paragraph 0031)* connected to said storage control device (*primary and secondary BIOS programs are executed by the CPU, paragraph 0011)*,

Lin does not explicitly teach a storage system wherein said CPU of said storage control apparatus executes the update of said BIOS by writing to said memory in standby; wherein said service processor of said storage control apparatus permits the switching of said memory in standby to said memory in operation when the update of said BIOS in said memory in standby succeeded; and wherein said CPU of said storage control apparatus writes the BIOS of said memory switched to operation, to said memory switched to standby for redundancy after said switching.

Tamori et al. disclosed the method of updating a program and information processing system by configuring a flash ROM board as two banks A and B (*col. 5 lines 49-55).* Updating a BIOS in the flash ROM board, is described in fig. 8, utilizing the flash ROM board with two banks and the bank change circuit (*fig. 6, 92, col. 6 lines 11-17)* where the new BIOS is supplied from the network interface card to the RAM (*fig. 8, s9, col. 6 lines 35-39)* and the content of RAM is then written to bank A (*fig. 10-18).*

Refer to claim 1 for motivational statement.

In regard to claim 21, Lin disclosed the storage system according to claim 20, wherein said service processor of said storage control apparatus switches said permitted memory in

standby to a memory in operation (*If the primary BIOS program is corrupted, the computer system will automatically switch over to the secondary BIOS program, paragraph 0030)*, and said memory in operation to said memory in standby when said hardware is started up (*POST power-on-self-test allows primary BIOS program to test determine if it is functional, paragraph 0031).*

In regard to claim 23, Lin disclosed the storage system according to claim 19, wherein said CPU of said storage control apparatus prevents switching said memory in standby to the memory in operation when the update of said BIOS in said memory in standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 24, Lin disclosed the storage system according to claim 19, wherein said CPU of said storage control apparatus prevents switching said memory switched to standby, to said memory in operation, when writing of said BIOS in said memory switched to standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 25, Lin disclosed the storage system according to claim 19, further comprising another storage control apparatus, which is connected to said storage devices and said storage control apparatus and for controlling said storage devices, wherein said storage control apparatus executes the update of the BIOS in the memory in standby of said other storage

control apparatus according to the update of the BIOS in said memory in standby of said storage control apparatus (*recovery of BIOS by overwritten the secondary BIOS with a copy of the functional primary BIOS, paragraph 0050).*

In regard to claim 26, Lin disclosed the storage system according to claim 19, further comprising another storage control apparatus, which is connected to said storage devices and said storage control apparatus and for controlling said storage devices, wherein said storage control apparatus executes the synchronization processing of the BIOS with said other storage control apparatus (*pure copying operation performed to place an identical copy of the primary BIOS into secondary BIOS, paragraph 0050).*

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Cepulis et al. (US 2004/0025002).

In regard to claim 29, Cepulis et al. disclosed a redundant management method for BIOS, comprising the steps of;

Booting updated BIOS in a first memory (*boot manager may force a cold boot or restart of the computer system so that the newly updated BIOS will be executed, paragraph 0043)*; and

Copying the updated BIOS in the first memory to a second memory that stored BIOS before said updating after said booting (*if a change to the system BIOS is detected, the back-up driver or the boot manager may be adapted to create a back-up of the system BIOS when the system BIOS is change, fig. 3, 304, paragraph 0046).*

In regard to claim 30, Cepulis et al. disclosed a data processing apparatus, comprising:

A hardware including a CPU (*processor, fig. 1, 102)*;

A pair of memories which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware (*BIOS and back-up BIOS, fig. 2, 200, 202)*; and

Wherein said CPU boots an updated BIOS in one of said pair of memories and copies said updated BIOS in the said one of said pair of memories to the other memory before said updating after said booting (*if a change to the system BIOS is detected, the back-up driver or the boot manager may be adapted to create a back-up of the system BIOS when the system BIOS is change, fig. 3, 304, paragraph 0046).*

In regard to claim 31, Cepulis et al. disclosed a storage system, comprising:

A storage control apparatus comprises:

A hardware including a CPU (*processor, fig. 1, 102);*

A pair of memories which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware (*BIOS and back-up BIOS, fig. 2, 200, 202)*; and

A plurality of storage devices (*BIOS and back-up BIOS, fig. 2, 200, 202)* connected to said storage control device (*boot manager, fig. 2, 206)*,

Wherein said CPU boots an updated BIOS in one of said pair of memories (*boot manager may force a cold boot or restart of the computer system so that the newly updated BIOS will be executed, paragraph 0043)* and copies said updated BIOS in the said one of said pair of memories to the other memory before said updating after said booting (*if a change to the system BIOS is detected, the back-up driver or the boot manager may be adapted to create a back-up of the system BIOS when the system BIOS is change, fig. 3, 304, paragraph 0046).*

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LOAN TRUONG whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SCOTT BADERMAN can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
Patent Examiner
Art Unit: 2114

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER